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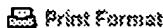
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Alexandre Eichenberger, Waleed Meleis, Suman Maradani

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Kanna Shimizu, David L. Dill

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This paper presents novel uses of functional interface specifications for verifying RTL designs. We demonstrate how a simulation environment, a correctness checker, and a functional coverage metric are all created automatically from a single specification. Additionally, the process exploits the structure of a specification written with simple style rules. The methodology was used to verify a large-scale I/O design from the Stanford FLASH project.

Keywords: BDD minimization, coverage, input generation, testbench**4** [Accurate and efficient predicate analysis with binary decision diagrams](#)

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